Jaewoong Sim

CONTACT INFORMATION

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RESEARCH INTERESTS

- Computer architecture and systems, with a focus on the interaction between microarchitecture, compilers, and operating systems.
- Accelerator architectures for machine learning.
- Die-stacked memory architectures and emerging technologies.
- Parallel architectures and embedded systems for emerging large-scale and mobile applications.

EDUCATION

2009-2015 **Georgia Institute of Technology** Atlanta, GA

Ph.D., Electrical and Computer Engineering August 2015

- Advisor: Hyesoon Kim
- Thesis: Architecting Heterogeneous Memory Systems with 3D Die-Stacked Memory

M.S., Electrical and Computer Engineering December 2010

Seoul National University Seoul, South Korea

B.S. with Honors, Electrical Engineering February 2007

PUBLICATIONS

PACT 2015 Joo Hwan Lee, **Jaewoong Sim**, and Hyesoon Kim, "BSSync: Processing Near Memory for Machine Learning Workloads with Bounded Staleness Consistency Models," Proc. of 24th International Conference on Parallel Architectures and Compilation Techniques, San Francisco, CA, October 2015.
Won Best Paper Award

MICRO 2014 **Jaewoong Sim**, Alaa R. Alameldeen, Zeshan Chishti, Chris Wilkerson, and Hyesoon Kim, "Transparent Hardware Management of Stacked DRAM as Part of Memory," Proc. of 47th International Symposium on Microarchitecture, Cambridge, UK, December 2014.

IEEE MICRO Top Picks 2014 **Jaewoong Sim**, Gabriel H. Loh, Vilas Sridharan, and Mike O'Connor, "A Configurable and Strong RAS Solution for Die-Stacked DRAM Caches," IEEE Micro Special Issues: Top Picks from 2013 Computer Architecture Conferences, May/June 2014.

ISCA 2013 **Jaewoong Sim**, Gabriel H. Loh, Vilas Sridharan and Mike O'Connor, "Resilient Die-Stacked DRAM Caches," Proc. of 40th International Symposium on Computer Architecture, Tel-Aviv, Israel, June 2013.
Selected for IEEE Micro Top Picks '14

MICRO 2012 **Jaewoong Sim**, Gabriel H. Loh, Hyesoon Kim, Mike O'Connor and Mithuna Thottethodi, "A Mostly-Clean DRAM Cache for Effective Hit Speculation and Self-Balancing Dispatch," Proc. of 45th International Symposium on Microarchitecture, Vancouver, BC, Canada, December 2012.

ISCA 2012 **Jaewoong Sim**, Jaekyu Lee, Moinuddin K. Qureshi and Hyesoon Kim, "FLEXclusion: Balancing Cache Capacity and On-Chip Bandwidth via Flexible Exclusion," Proc. of 39th International Symposium on Computer Architecture, Portland, OR, June 2012.

PPoPP 2012 **Jaewoong Sim**, Aniruddha Dasgupta, Hyesoon Kim and Richard Vuduc, "A Performance Analysis Framework for Identifying Potential Benefits in GPGPU applications," Proc. of 2012 Symposium on Principles and Practice of Parallel Programming, New Orleans, LA, February 2012.

PATENTS

[P1] Method and Apparatus for Implementing a Heterogeneous Memory Subsystem. Christopher B. Wilkerson, Alaa R. Alameldeen, Zeshan A. Chishti, and Jaewoong Sim. US Patent Pub. No. 2015/0278091.

[P2] Memory Scheduling for RAM Caches Based on Tag Caching. Gabriel H. Loh and Jaewoong Sim. US Patent Pub. No. 2014/0181384.

[P3] Dirty Cacheline Duplication. Gabriel H. Loh, Vilas K. Sridharan, James M. O'Connor, and Jaewoong Sim. US Patent Pub. No. 2014/0173379.

[P4] Partitioning Caches for Sub-Entities in Computing Devices. Gabriel H. Loh and Jaewoong Sim. US Patent Pub. No. 2014/0173211.

[P5] Bypassing Memory Requests to a Main Memory. Jaewoong Sim and Gabriel H. Loh. US Patent Pub. No. 2014/0164713.

[P6] Dynamically Configuring Regions of a Main Memory in a Write-Back Mode or a Write-Through Mode. Jaewoong Sim, Mithuna S. Thottethodi, and Gabriel H. Loh. US Patent Pub. No. 2014/0143505.

[P7] Predicting Outcomes for Memory Requests in a Cache Memory. Gabriel H. Loh and Jaewoong Sim. US Patent Pub. No. 2014/0143502.

[P8] Bypassing a Cache when Handling Memory Requests. Gabriel H. Loh, Jaewoong Sim, and James M. O'Connor. US Patent Pub. No. 2014/0143493.

TECHNICAL DOCUMENTATION (REFERRED)

Hyesoon Kim, Jaekyu Lee, Nagesh B. Lakshminarayana, **Jaewoong Sim**, Jieun Lim, and Tri Pho, "MacSim: A CPU-GPU Heterogeneous Simulation Framework," Georgia Institute of Technology, 2012.

RESEARCH EXPERIENCE

September 2015 - Current **Intel Labs** Hillsboro, OR

Research Scientitst, Accelerator Architecture Lab (AAL)

- Manager: Deborah T. Marr
- Defining accelerator architecture and systems for machine learning

June 2013 - December 2013 **Intel Labs** Hillsboro, OR

Research Intern, Microarchitecture Research Lab (MRL)

- Manager: Shih-Lien Lu

- Mentors: Chris Wilkerson, Alaa R. Alameldeen, and Zeshan Chishti
- Research on using die-stacked DRAM as part of main memory via hardware management.
- Papers published in MICRO 2014 and submitted to journal. One U.S. patent filed [P1].

January 2012 - August 2012 **AMD Research** Bellevue, WA

Research Intern, AMD Research Lab

- Mentor: Gabriel H. Loh
- Designing practical, scalable die-stacked DRAM cache architectures [MICRO 2012].
- Providing efficient reliability support for die-stacked DRAM caches [ISCA 2013] [IEEE MICRO TOP PICKS 2014].
- Seven U.S. patents filed [P2, P3, P4, P5, P6, P7, P8].

January 2011 - August 2015 **Georgia Institute of Technology** Atlanta, GA

Graduate Research Assistant, HPArch Lab

- CPU/GPU performance modeling and benefit analysis [PPoPP 2012].
- Impact of cache inclusion properties on CMPs with on-chip networks [ISCA 2012].
- HW/OS cooperative management of die-stacked memory under over-committed memory scenarios [In Submission].
- Architectural support for machine-learning workloads using iterative convergent algorithms [In Submission].
- Efficiently architecting phase change memory for approximate computing [In Submission].

January 2007 - July 2007 **Seoul National University** Seoul, South Korea

Research Assistant, Nano/Micro Systems and Controls (NMSC) Lab

- Worked in the Robot Sensor Group. Developed sensor device drivers for Linux.
- Conducted research on efficient motion detecting algorithms for inertial sensors.

WORK EXPERIENCE

October 2007 - June 2008 **SML Electronics Inc. (Startup Founded by NMSC Lab in SNU)** Seoul, South Korea

Project Manager

- Worked as a lead engineer in applying MEMS accelerometers to mobile devices.
- Designed a motion library and robot control & trajectory display software.

January 2002 - July 2005 **Mococo Inc.** Seoul, South Korea

Software Engineer

- Worked as a system programmer in developing Samsung Palm OS-based smartphone SPH-i550 and Motorola E310 (device drivers, system libraries and applications).
- Developed WINY/REXY GUI platforms for embedded OSes.
- Developed boot loaders for embedded processors including Samsung's S3C2410 and S3C2440.

Summer 2001 **Neowiz Corporation** Seoul, South Korea

Software Intern

- Designed a game engine library using C++ and Python.
- Developed an online multiplayer Tetris game (production-level code).

TEACHING EXPERIENCE

Georgia Institute of Technology Atlanta, GA

Graduate Teaching Assistant

- ECE 6100 - Advanced Computer Architecture **Fall 2010**
- CS 8803 - Languages and Compilers for Embedded Systems **Summer 2009**

Held office hours, led discussions, and graded homework/projects/exams (ECE 6100, CS 8803). Designed part of course projects and exams (CS 8803).

AWARDS & HONORS

Best Paper Award at PACT 2015	2015
IEEE Micro Top Picks in Computer Architecture	2014
Outstanding Graduate Research Assistant Award, Georgia Institute of Technology	2014
Bronze medal, EE Fair 2006, Seoul National University	2006
Seoul National University Scholarship	1999-2001, 2005-2006
Nestle Korea Ltd. Fellowship	2000

SOFTWARE

MacSim — MacSim is a cycle-level simulator for computer architecture research. It uses x86 and NVIDIA PTX instruction traces to simulate architectural behaviors including pipeline stages, multi-threading, and memory systems. I am one of the main developers and maintain the codebase.

GPUPerf — GPUPerf is a framework for identifying potential benefits in GPGPU applications. It quantitatively estimates potential performance benefits along four dimensions—inter-thread instruction-level parallelism, memory-level parallelism, computing efficiency, serialization effects—and helps programmers tune code for GPGPU platforms.

PROFESSIONAL ACTIVITIES

Program Committee, 2016 International Symposium on Microarchitecture (MICRO-49)

External Review Committee, 2016 International Symposium on Computer Architecture (ISCA-43)

Publicity Chair, 2015 International Symposium on Workload Characterization (IISWC 2015)

Reviewer of ACM Transactions on Architecture and Code Optimization (TACO)

Reviewer of IEEE Transactions on Very Large Scale Integration Systems (TVLSI)

Reviewer of IEEE Computer Architecture Letters (CAL)

External Reviewer of ISCA, MICRO, HPCA, ASPLOS

Organizing Committee, 2015 Georgia Tech Computer Architecture Conference (ArchiTECH 2015)

Student Volunteer, 2010 International Symposium on Microarchitecture (MICRO-43)

Tutorial Presenter, Ocelot and SST-MacSim Simulator in ICPADS 2013

Member of IEEE and ACM

REFERENCES

Available upon request